

I Want to Use an FPGA Before an ASIC. Can It Be One Patent?

This Patent Stuff and My Semiconductor Business – Part 14

Welcome to this post about patents and chips. Not a lot has been written about this combination, but there is a lot to know, especially for the innovators and entrepreneurs themselves. In this three-weekly series, I talk about various aspects, from my dual points of view of a patent agent and a semiconductor entrepreneur. If you like the article and read it on LinkedIn, give it a thumbs up, and/or click on Follow. If you like to work with us for your next patent, "contact us" info is on www.icswpatent.com. You can also subscribe/unsubscribe for short email alerts when the next post is available.

One characteristic of chip design innovations is that there are so many ways that you can implement something. One implementation may not even look like another one, and still use the same—new—method. How does that work for patents? Do you need to file a thousand patents for a thousand different implementations?

If your patent application is written broadly, one patent can cover many implementations. All patent lawyers and agents know that, and many inventors know it. Nevertheless, many chip patents are unnecessarily narrow – just because the guy who wrote it had no clue what the invention actually was. Chip designs usually come with a high degree of expertise, and even though the inventor often documents what (s)he has implemented, (s)he often does not document the what or why behind it. When the patent guy just takes it without a full analysis (those who charge \$500 per hour can hardly justify spending time on an analysis, can they?) it results in a patent application that describes just one implementation. Perhaps hierarchically, but still one implementation. The real invention may be up for grabs.

So, your patent practitioner needs to love the technology and be discourteous enough to ask the inventor what he or she really meant, how he/she really did it, why it works, where else it can be applied, and how else it could be implemented. A good practitioner may know quite a bit about the latter, but must still fully (FULLY!!) understand the invention and the technology to write a proper application.

For digital systems, it sometimes results in a single architecture that does the trick, or a couple of variations. There will still be possibilities to implement some blocks as hardwired circuits, or as dedicated DSPs, or as firmware executed on a general-purpose processor. There may be variations as to what is included inside a chip and what may be elsewhere. The same RTL may be implemented on an FPGA or an ASIC. So yes, if written properly, one patent application can cover both.



**Your patent
practitioner
needs to be
discourteous
enough!**

It gets trickier when the invention is not on the architectural level, but on the digital circuit level. Or on the architectural level including some blocks that can be expressed as simple gates or circuits, an AND gate, an OR gate, etc. It's so easy to draw and write about an AND gate. But how often are you actually using AND gates in an ASIC? More likely that it will be a NAND or NOR gate. Or a bunch of them. Your logic is probably synthesized, so you may not even know what you'll end up with. The description of the invention needs to describe and claim all possibilities, otherwise, again, you're giving away the invention.

For mixed-signal circuits it gets even more elaborate. Not only can some of the functionality be implemented in analog, digital, or firmware; the analog circuits may have endless possibilities for variation. Unless you want to do a lot of handholding, the patent practitioner needs to be able to come up with, draw, and describe at least all the basic ones. Then there is the issue of claiming. Say you have an analog circuit, then there may be some transistors that are essential to the basic function, and other transistors that make it perform faster, more accurately, or at a lower power. This needs to be claimed hierarchically, where your base claim (the root of the hierarchical tree) may describe the netlist of the essential circuit (in one sentence). Then a list of dependent claims to describe the various branches. Some of the branches may describe circuits or blocks implemented in whole different technologies (analog versus digital versus firmware).

In some cases, it may be beneficial to integrate everything in one die, whereas in other cases you decide to use multiple dies, maybe in the same package, maybe piggybacking. Your patent application must foresee all those possibilities and claim them, or at least describe them, so that you can close the loopholes for your competitors.

So is it possible to cover the FPGA and ASIC implementations in one patent? Absolutely! Just make sure the damn patent guy understands you!

(Or lady, just in case.)

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